Monolithic GaAs HBT p-i-n Diode Variable Gain Amplifiers, Attenuators, and Switches

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***Abstract*—We report on monolithic circuits integrating HBT's and p-i-n diodes using a common HBT MBE structure. An HBT variable gain amplifier using a p-i-n diode as a variable resistor achieved a gain of 14.6 dB, a bandwidth out to 9 GHz, a gain control range of >15 dB, and an IP3 of 28 dBm. A two-stage HBT p-i-n diode attenuator from 1–10 GHz and an *X*-band one-pole two-throw HBT p-i-n diode switch were also demonstrated. The two-stage p-i-n attenuator has over 50 dB dynamic range at 2 GHz and a maximum IP3 of 9 dBm. The minimum insertion loss is 1.7 dB per stage and has a flat response to 10 GHz. The *X*-band switch has an insertion loss of 0.82 dB and an off-isolation of 25 dB. The bandwidth is greater than 35% and the IP3 is greater than 34.5 dBm. These circuits consist of p-i-n diodes constructed from the base-collector MBE layers of a base-line HBT process. This work demonstrates the first monolithic integration of p-i-n diode switch, variable gain control, and attenuation functions in an HBT technology without additional processing steps or MBE material growth.**

I. Introduction

THE use of p-i-n diodes in many microwave communication systems is attractive because of their high breakdown voltages, fast switching characteristics, and their variable resistance with bias. They provide circuit functions in broadband switches, attenuators, photodetectors, phase shifters, and variable gain amplifiers. Most uses of p-i-n diodes have been as discrete components integrated in a hybrid circuit. This makes it cumbersome for the designer because it involves a lot of bench testing/tuning to make the circuit work correctly.

In GaAs HBT technology, the p-i-n diode can be constructed from existing material layers, allowing the monolithic integration of p-i-n diodes with HBT transistors. The lightly doped collector layer of the HBT device structure can be used as the intrinsic layer of the p-i-n. The heavily doped base and subcollector act as the P^+- and N^+-type material. With no modification to the existing baseline HBT process, reasonable p-i-n diode performance can be achieved. Because the HBT and p-i-n diode structures are compatible, HBT technology offers additional circuit functionality at no added expense. This makes it attractive for commercial applications where cost is a major factor. For military applications where the performance of both HBT and p-i-n diodes are of major concern, an optimized p-i-n structure can be separately grown using selective MBE techniques, but at the expense of a more complex process.

Previous p-i-n diode integration in HBT technology has been demonstrated to construct monolithic p-i-n varactors for HBT VCO's [1] and p-i-n diode optical detectors for receivers [2]. However, there has been no previous reports of HBT p-i-n attenuator, switch, and variable-gain amplifier performance. This paper presents the performance of an HBT p-i-n diode 1–9 GHz wideband variable-gain amplifier, a 1–10 GHz p-i-n-variable attenuator, and an *X*-band one-pole two-throw p-i-n switch made from the intrinsic device layers of our baseline HBT process.

Manuscript received March 26, 1993; revised June 22, 1993.

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IEEE Log Number 9213001.

II. GaAs HBT Process Technology

The MBE profile of our standard GaAs HBT process is shown in Fig. 1. This profile incorporates a base thickness of 1400 Å uniformly doped to 1×10^{19} cm^{-3}, an N^- collector 7000 Å thick and lightly doped to 7×10^{15} cm^{-3}, and an N^+ subcollector doped to 5×10^{18} cm^{-3}. The lightly doped collector is used to construct the intrinsic layer of the p-i-n diode. The heavily doped base and subcollector constructs the P^+- and N^+-type layers of the p-i-n. The reverse breakdown voltage is greater than 20 V. The reverse bias capacitance per square micron of the p-i-n is 0.162 $fF/\mu m^2$ at full depletion, however, this does not include the lateral parasitic capacitances which are about twice the parallel diode depletion capacitance. The series on-resistance of the diode is 600 Ω-μm^2 and is mainly due to the ohmic contact resistance of the base and collector. The baseline HBT transistors have an f_t and f_{max} of 23 and 50 GHz, respectively, at a current density of 20 kA/cm^2. Fig. 2 shows f_t and f_{max} as a function of collector current for both 3×10 μm^2 and 2×10 μm^2 four-finger HBT transistors. This baseline process consists of a 2-μm emitter self-aligned base ohmic metal (SABM) HBT technology which incorporates nichrome 100 Ω/square TFR's, MIM capacitors, Schottky diodes, spiral inductors, backside vias, as well as the p-i-n diodes.

III. p-i-n Diode Model

The performance of the p-i-n diode is dependent on several factors involving the MBE layers. These layers are used in both the HBT transistor and the p-i-n diode.

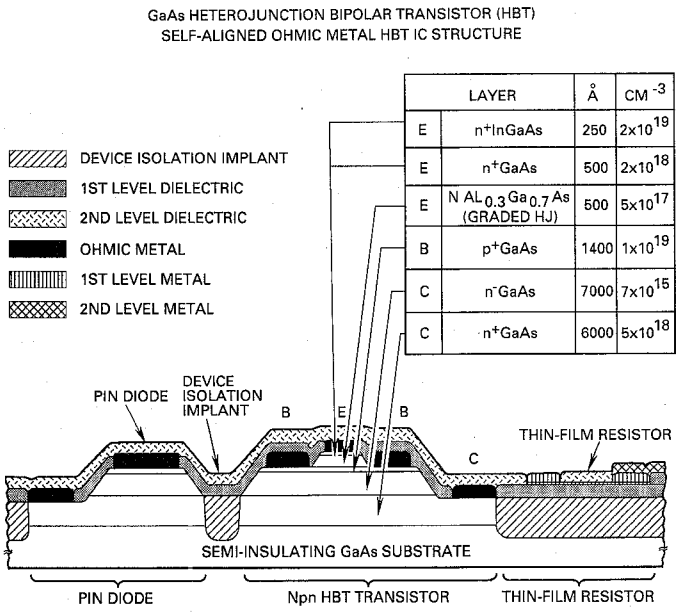


Fig. 1. HBT-p-i-n diode MBE profile.

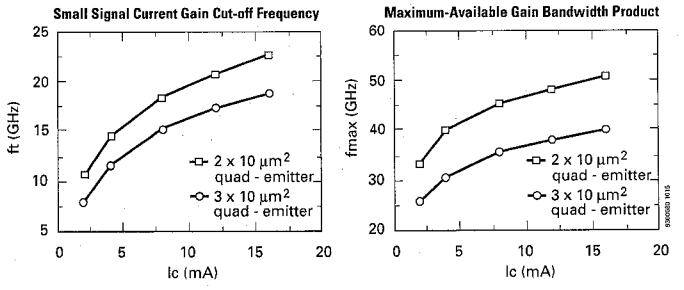


Fig. 2. F_t and F_{max} as a function of I_c for both a 3×10 μm^2 and 2×10 μm^2 quad-emitter transistor.

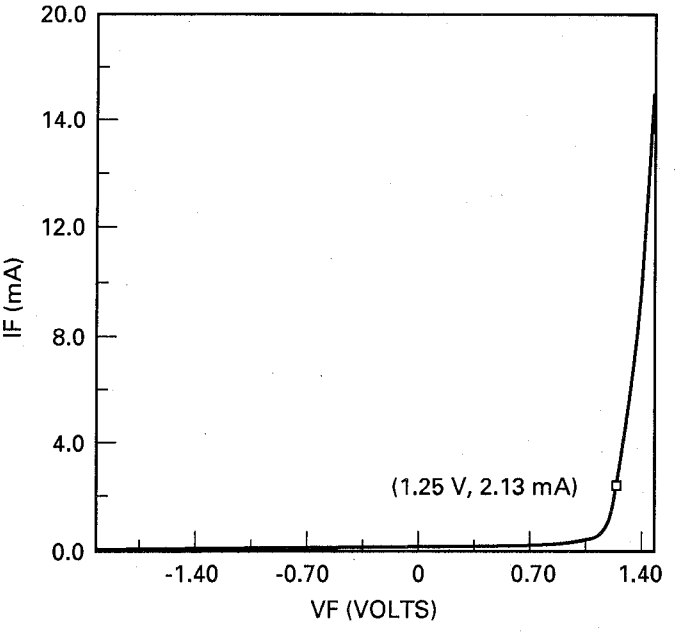


Fig. 3. HBT p-i-n diode dc I–V characteristics.

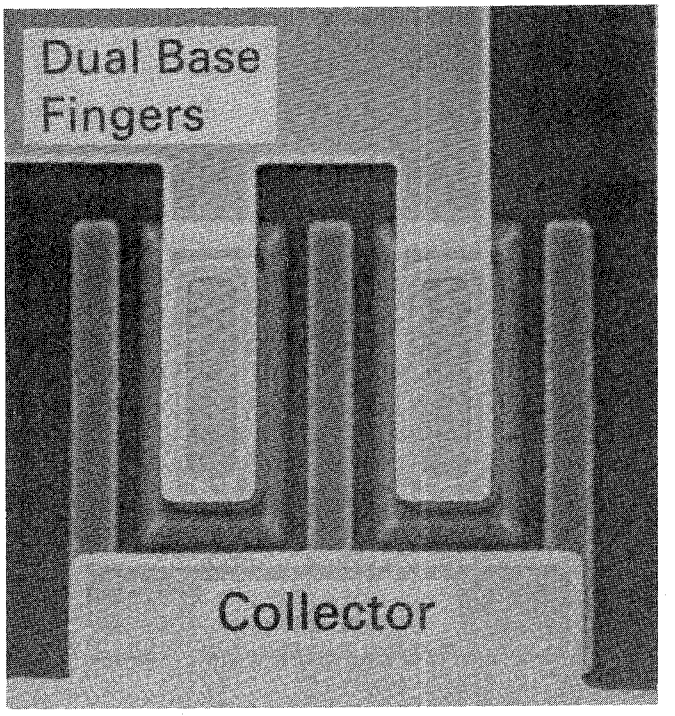
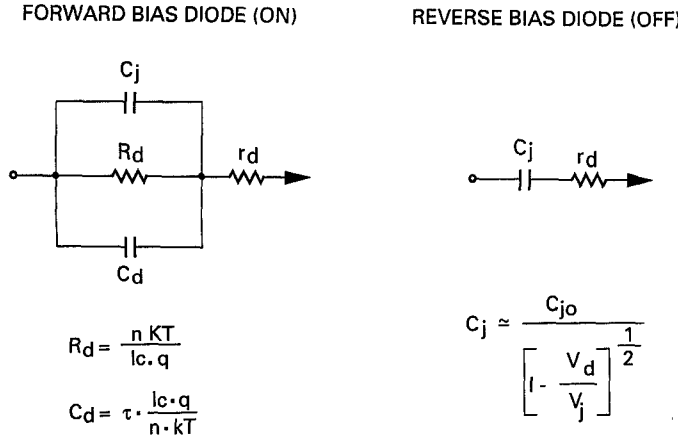


Fig. 4. SEM photograph of a 5×15 μm^2 dual-base finger p-i-n diodes.

The p-i-n diode device design trade-offs is described in greater detail, elsewhere [3]. The design trade-offs for the HBT–p-i-n diodes involve performance trade-offs in the HBT transistor in addition to the p-i-n diode. The advantages of the HBT device structure for the p-i-n diode is that the HBT device base is usually doped deep into degeneracy in order to achieve low lateral and ohmic contact base resistance. This improves the f_{max} of the HBT devices. It also improves the on-resistance of the p-i-n diode. The wide and very lightly doped collector gives the p-i-n diode a low series off-capacitance. It also gives the HBT transistor a low collector-base capacitance which reduces the Miller effect. In addition to reducing the capacitance, a wider collector will increase the breakdown voltage, however, this will degrade the f_t performance of the HBT device. Thus, optimization of both HBT device and p-i-n diode MBE layers depends on the performance requirements of the circuit application. In this paper, we report the p-i-n diode circuit performance of our base-line HBT material and process.

A p-i-n diode model was derived using both dc and small-signal s-parameters. A typical I–V curve of a 5×5 μm^2 dual base finger p-i-n diode is shown in Fig. 3. The ideality factor of the HBT p-i-n diode was found to be about 2.03. Fig. 4 shows a photograph of a 5×15 μm^2 dual base finger p-i-n diode. The diode has an interdigitated base finger layout which closely resembles the HBT transistor layout. This type of layout has a significant amount of side-wall capacitance associated with it, compared to the geometrically round or donut-shaped diode layouts. The parasitic off-capacitance is about two times the calculated parallel plate capacitance defined by the base mesa.

The small-signal modeling of the HBT p-i-n diode was



MODEL PARAMETER	SYMBOL	VALUE
SERIES CONTACT RESISTANCE	r_d	3.5-4Ω
ZERO BIAS DEPLETION JUNCTION CAPACITANCE	C_{jo}	0.097 pF
JUNCTION POTENTIAL	V_j	0.356V
GRADING COEFFICIENT	M	0.5
IDEALITY FACTOR	n	2.03
SATURATION CURRENT	I_s	6.58×10^{-14}A
REVERSE BREAKDOWN VOLTAGE	V_{BR}	>20V
TRANSIT TIME	τ	0.43 ps

Fig. 5. HBT p-i-n diode model.

done over the forward bias region and a forward bias model was derived. The reverse bias model was obtained by small-signal extraction of the reverse bias capacitance at zero bias. Since calculations show that the p-i-n diode is almost fully depleted at zero bias, about 5/7 depleted, the zero bias capacitance was used with the assumption of a 35% reduction in value for full reverse bias depletion. Fig. 5 shows the forward and reverse bias model of a 5×15 μm^2 dual base finger p-i-n diode. In the forward bias operation, the dynamic conductance is a function of current given by

$$G_d = I_c \cdot q/(n \cdot kT)$$

where n is the ideality factor. The parallel diode diffusion capacitance is approximately given by

$$C_d \approx T_{au} \cdot G_d.$$

T_{au} was imperically extracted from the small-signal modeling over bias current. The series ohmic contact resistance r_d was also obtained from small-signal modeling. The small signal p-i-n diode model of this work was used for the HBT p-i-n VGA, the p-i-n attenuator, and the SPDT *X*-band p-i-n switch designs with good success. A spice macromodel for p-i-n diodes was recently reported [4]. This model imperically models the p-i-n diode impedance as well as the transient characteristics.

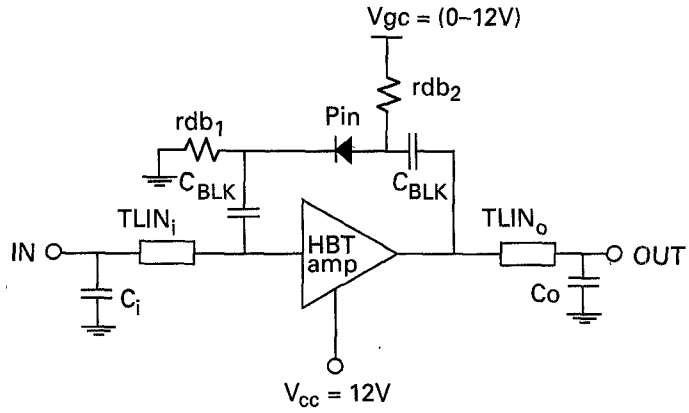


Fig. 6. Schematic of the HBT p-i-n diode variable gain wideband amplifier.

IV. HBT p-i-n Diode Variable Gain Amplifier

Typical p-i-n diode variable gain amplifiers use p-i-n diodes as variable resistors in either the series or parallel feedback path of a common emitter (source) amplifier. This is a normal practice in MIC-hybrid design. For the first time, p-i-n diodes are integrated monolithically on GaAs to perform the same function, but without the problems incurred in assembling a hybrid. By integrating the p-i-n diode on-chip, the size and complexity of the circuit can be reduced.

The schematic of the HBT p-i-n diode variable gain wideband amplifier developed in this work is shown in Fig. 6. Parallel feedback integration of the p-i-n diode was chosen in order to obtain broadband gain performance. The parallel diffusion capacitance of the p-i-n diode shunts the variable dynamic diode resistance and consequently, limits the gain bandwidth over the gain control range. This effect is less pronounced when applying the p-i-n diode as parallel feedback. For wideband response, the basic Darlington feedback amplifier topology was chosen. The Darlington amplifier has been previously demonstrated in HBT technology [5]. The Darlington amplifier is well suited for this application because it is compact, achieves wide bandwidths, incorporates parallel feedback, and can maintain good input and output VSWR's over a large range of feedback resistance. Simple microstrip tuning networks are provided at the input and output to enhance the VSWR's. A photograph of the fabricated HBT p-i-n diode VGA is illustrated in Fig. 7. The total chip size is 0.5×1.1 mm^2.

Excellent bandwidth and gain control were measured. Fig. 8 shows the variable gain performance of the wideband VGA. The nominal gain is 14.6 dB while the upper 3-dB band edge is 9 GHz. Fig. 9 illustrates the gain as a function of voltage control at 5 GHz. The variable gain control range is ≥ 15 dB with a gain control voltage range from 0–12 V. The maximum current through the p-i-n diode is 6 mA. The nominal supply voltage to the Darlington amplifier is 12 V with a current draw of 41 mA. The voltage at the collectors of the Darlington pair is 4.0 V. An ac/dc load resistor drops 8 V from the supply to the collectors. For lower power dissipation, a spiral in-

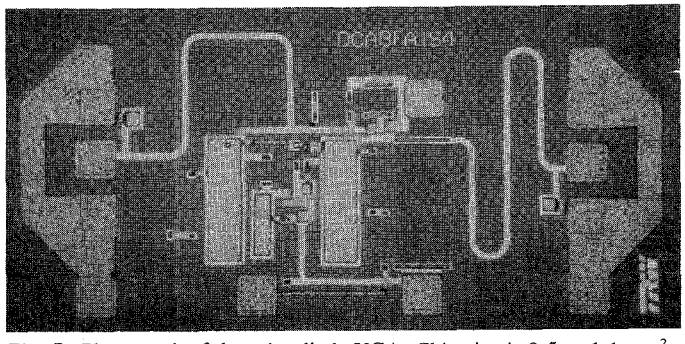


Fig. 7. Photograph of the p-i-n diode VGA. Chip size is 0.5 × 1.1 mm^2.

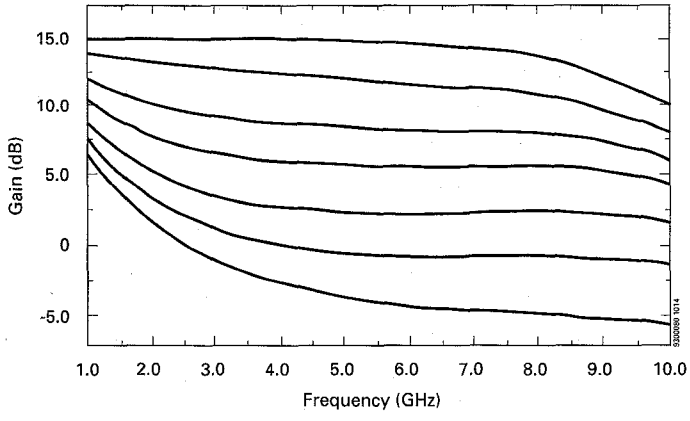


Fig. 8. Wideband variable gain performance.

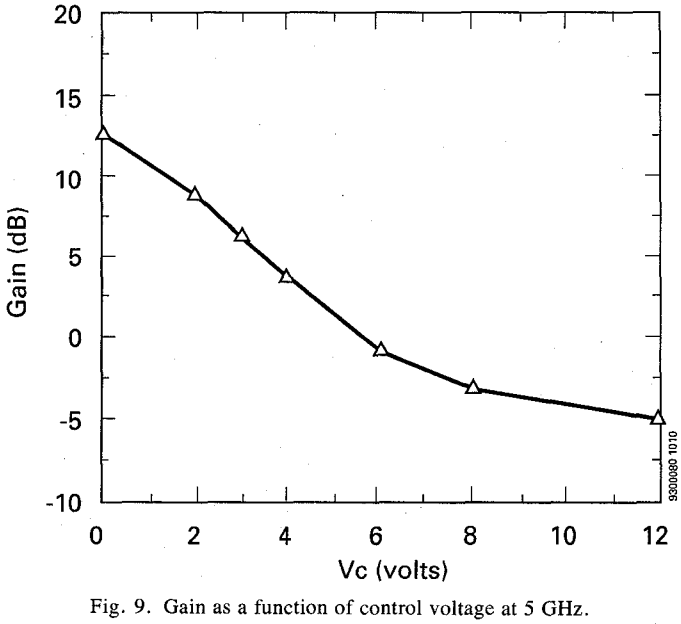
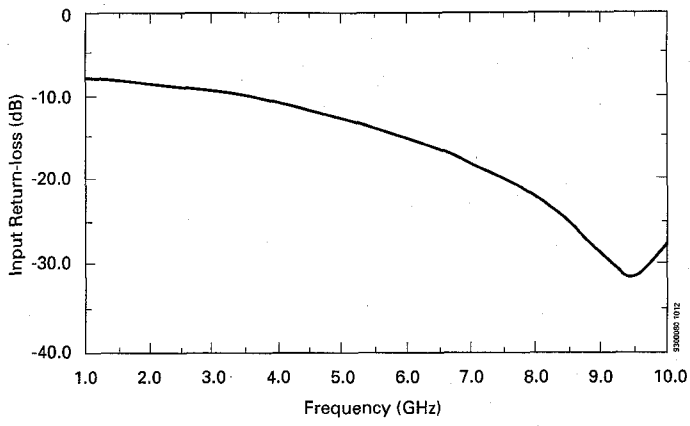


Fig. 9. Gain as a function of control voltage at 5 GHz.



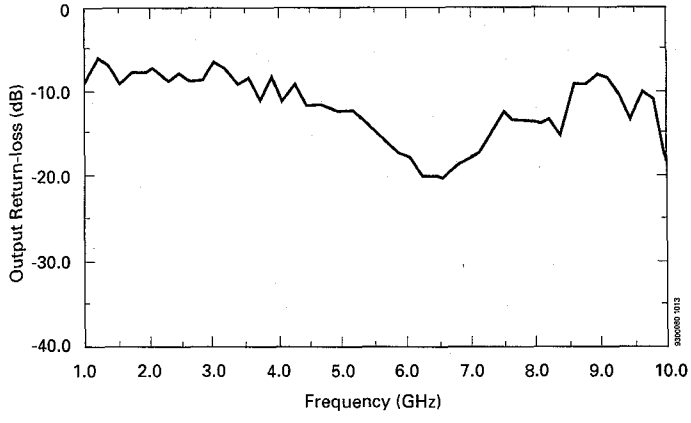


Fig. 10. Return-loss performance at maximum gain setting.

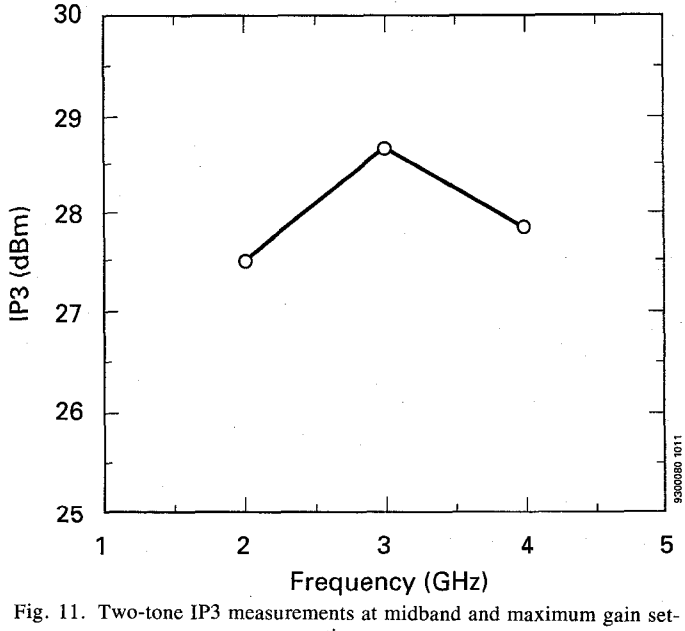


Fig. 11. Two-tone IP3 measurements at midband and maximum gain setting.

ductor can replace the load resistor providing a more efficient biasing scheme at the expense of chip real estate. The bandwidth response maintained its flatness through the gain control range. The lower band edge gain rolls up due to the two dc blocking capacitors on either side of the p-i-n diode. This lower gain roll-up can be shifted down in frequency by employing off-chip capacitors in parallel with the on-chip feedback blocking capacitors. Fig. 10 shows the return losses of the VGA at maximum gain setting. The IP3 was measured at maximum gain setting at midband and is illustrated in Fig. 11. The IP3 is $\geq$28 dBm with a IP3/dc power ratio of 3.8 which is calculated assuming 4 V on the collector. This IP3 efficiency performance ratio is about 3–4 times less than a previously

reported 5–11 GHz HBT balanced amplifier which achieves a ratio 13.5 [6]. The lower IP3 performance of the HBT p-i-n VGA is due to its less efficient Darlington feedback configuration. The VGA however, can achieve multioctave bandwidth performance with 15 dB of gain control range.

The HBT variable gain amplifier implements gain control capability with the use of monolithically integrated p-i-n diodes which has not been previously demonstrated.

V. p-i-n Diode Attenuator

P-i-n diodes are convenient for constructing attenuators because of the diode's resistive characteristics as a function of bias. There are several conventional attenuator topologies which are typically constructed with discrete components and may involve complex driver circuits as well as slope compensation [7]–[11]. Monolithic integration of p-i-n attenuator functions with HBT IC's can reduce the size, complexity, and assembly cost of multifunctional architectures. The following section describes the design of a simple attenuator circuit based on the HBT p-i-n diodes.

The schematic of the two-stage p-i-n diode attenuator is shown in Fig. 12. The single-stage p-i-n diode attenuator circuit consists of a series and a shunt diode to form a T-network. The T-network was used in order to obtain a combination of good insertion loss and attenuation range. The low-frequency response is limited by the 15 pF blocking capacitors. In this design the series and shunt diodes are biased through a range of forward biases. The diodes are never fully reverse biased. A fixed supply of 12 V and a variable attenuation voltage ranging from 0–12 V was used. A maximum current of 6 mA was measured for the diodes in the forward bias state for each stage. A photograph of the 2-stage p-i-n diode attenuator circuit is shown in Fig. 13. This chip measures 1.2 × 1.8 mm^2.

The variable attenuation performance from 0.05–10 GHz is shown in Fig. 14. The minimum insertion loss is 3.4 dB for two stages. This comes out to 1.7 dB insertion loss for a single stage and is typical of commercially available hybrid p-i-n variable attenuators ($\approx$2 dB) that achieve smaller bandwidths using this topology. The graph in Fig. 14 shows insertion loss response over the full band for $\approx$5 dB steps at 2 GHz. The insertion loss flatness becomes compromised at the higher attenuation states because the shunt and series diodes are under forward bias where the diffusion capacitance shunts the dynamic resistance at higher frequencies. This gives the positive slope in the response. The low-end cutoff is due to the size of the blocking capacitors used. The low-end response could be extended by incorporating larger off-chip capacitors in parallel with the on-chip capacitors. Fig. 15 shows the return loss performance over the attenuation range. The input and output return losses are maintained at about 10 dB and are fairly insensitive over the attenuation range. Fig. 16 shows modeled vs. measured

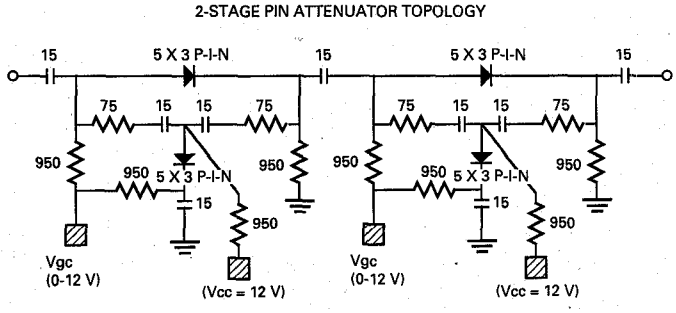


Fig. 12. Schematic of the two-stage HBT p-i-n diode attenuator.

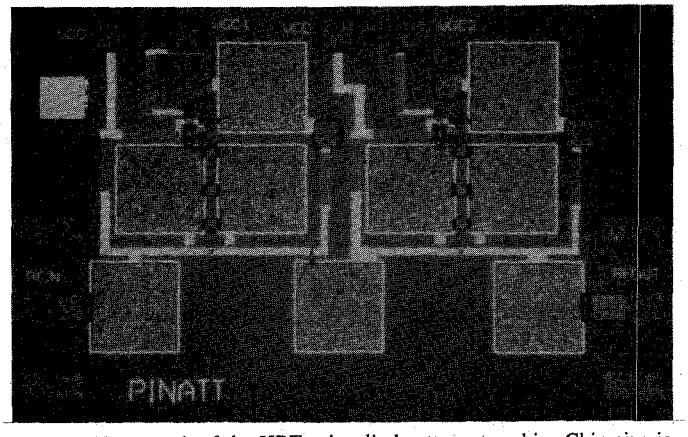


Fig. 13. Photograph of the HBT p-i-n diode attenuator chip. Chip size is 1.2 × 1.8 mm^2.

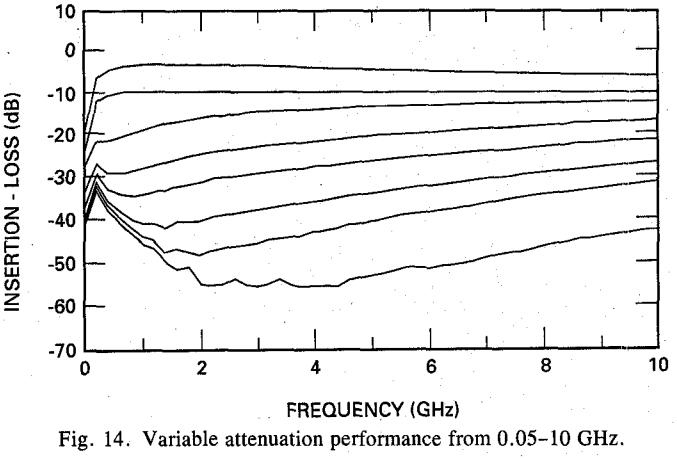


Fig. 14. Variable attenuation performance from 0.05–10 GHz.

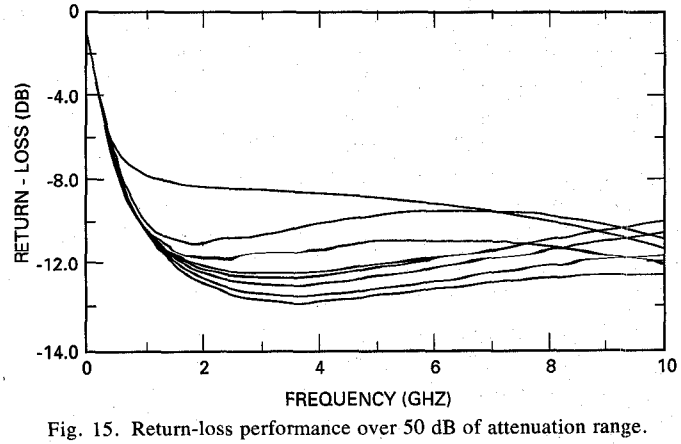


Fig. 15. Return-loss performance over 50 dB of attenuation range.

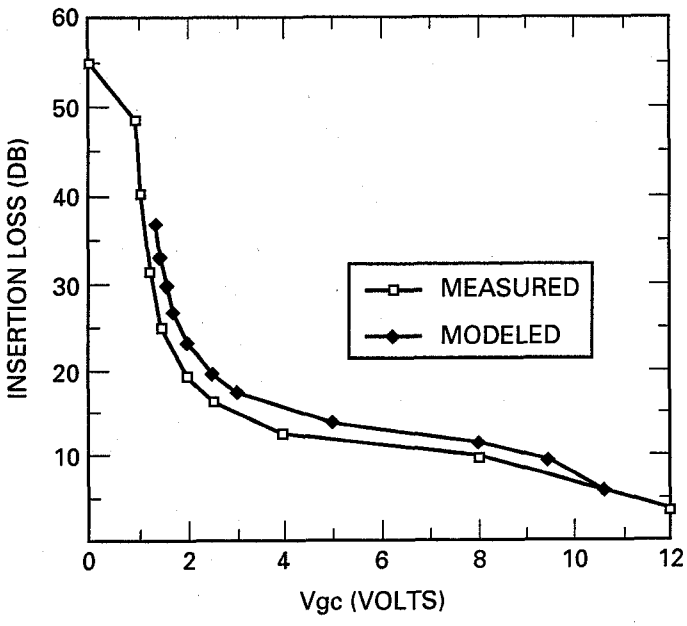


Fig. 16. Measured and modeled insertion loss as a function of voltage control at 2 GHz.

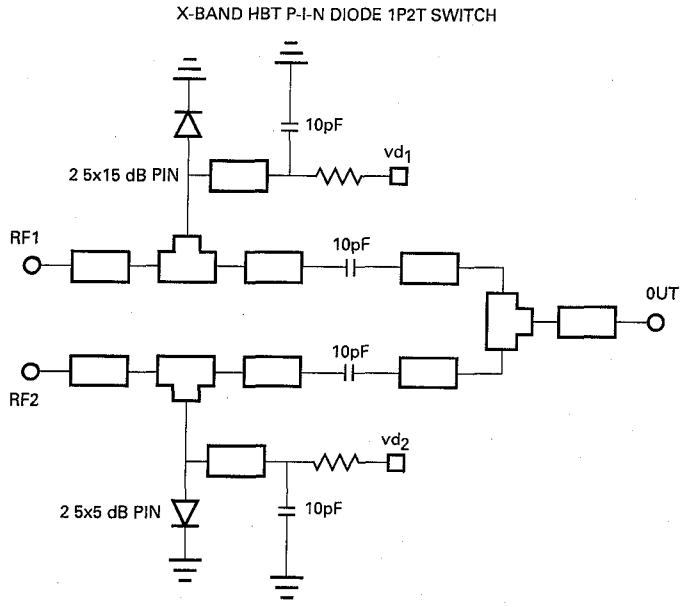


Fig. 17. Schematic of the 1P2T *X*-band p-i-n diode switch.

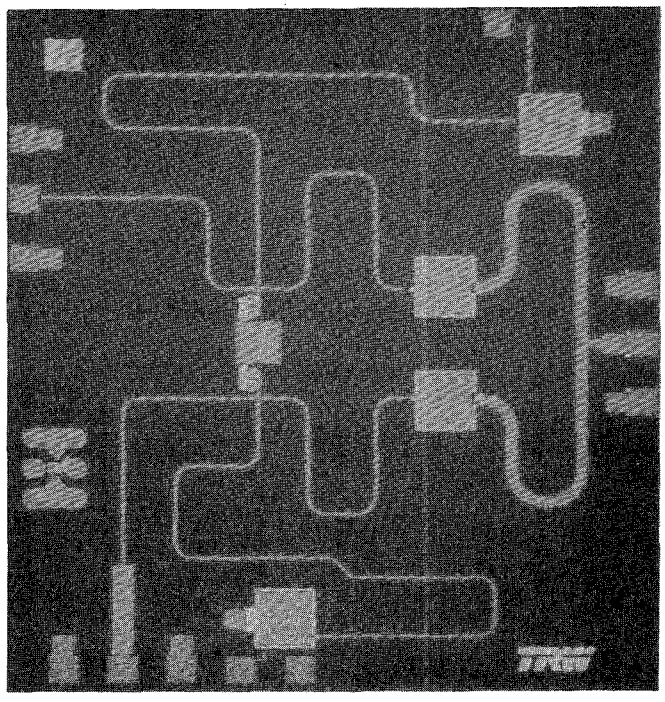


Fig. 18. Photograph of the 1P2T *X*-band p-i-n diode switch. Chip size is 2.4 × 2.4 mm^2.

insertion loss as a function of voltage, V_{gc}, at 2 GHz. The general voltage control characteristics agree over the attenuation range. The dynamic range at 2 GHz is greater than 50 dB. Thus, a single stage has 25 dB of variable attenuation. Typical p-i-n attenuators of this topology achieve 18–25 dB for a single stage.

IP3 of about 9 dBm was measured from 2–4 GHz at minimum insertion loss. The low IP3 is mainly due to the soft forward bias of the on-series diodes and the lack of full reverse bias of the off-shunt diodes. By further forward biasing the series diodes and reverse biasing the shunt diodes, the IP3 was improved by about 5 dBm. At the higher attenuation states, the IP3 degrades more because both shunt and series diodes are softly forward biased. The biasing scheme could be redesigned in order to obtain higher IP3 at the expense of more power consumption.

A. X-Band One-Pole Two-Throw Switch

P-i-n diodes are used as switches because of their compact size, high frequency and power handling capability [12]–[15]. They are often used in transceiver systems where high frequency and power are main performance drivers. For this reason, the monolithic integration of p-i-n diodes can be very useful in HBT technology.

An SPDT *X*-band p-i-n diode switch was developed to demonstrate the ability to integrate p-i-n diode switch functions in an existing HBT technology. A circuit schematic of a single-pole two-throw microwave switch is shown in Fig. 17. Each arm of the switch consists of two 5 × 15 μm^2 dual base shunt p-i-n diodes in parallel. The shunt configuration has the advantage of reliable thermal performance (lower thermal resistance). Quarter-wavelength lines transform the low impedance "on" diode to a high impedance at the output port for good isolation. Quarter-wave transformers are also used as *rf* chokes in the bias network of each p-i-n diode arm. MIM capacitors were used to terminate the quarter-wave lines instead of radial stubs in order to suppress coupling which could degrade the off isolation. A photograph of the p-i-n diode *X*-band switch is shown in Fig. 18. The chip area is 2.4 × 2.4 mm^2.

A plot of the insertion loss and isolation is shown in Fig. 19. The insertion loss is 0.82 dB at 10 GHz. An insertion loss of 1.3 dB has previously been achieved at *X*-band using monolithically integrated p-i-ns in a GaAs

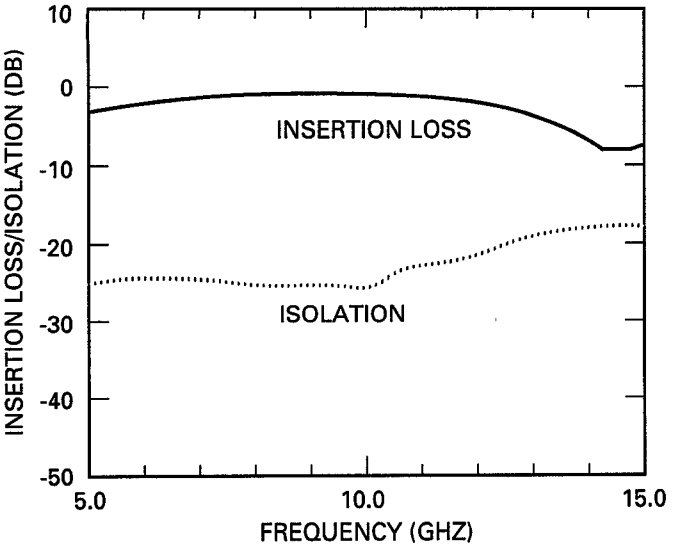


Fig. 19. Insertion loss and off-isolation performance of the *X*-band switch.

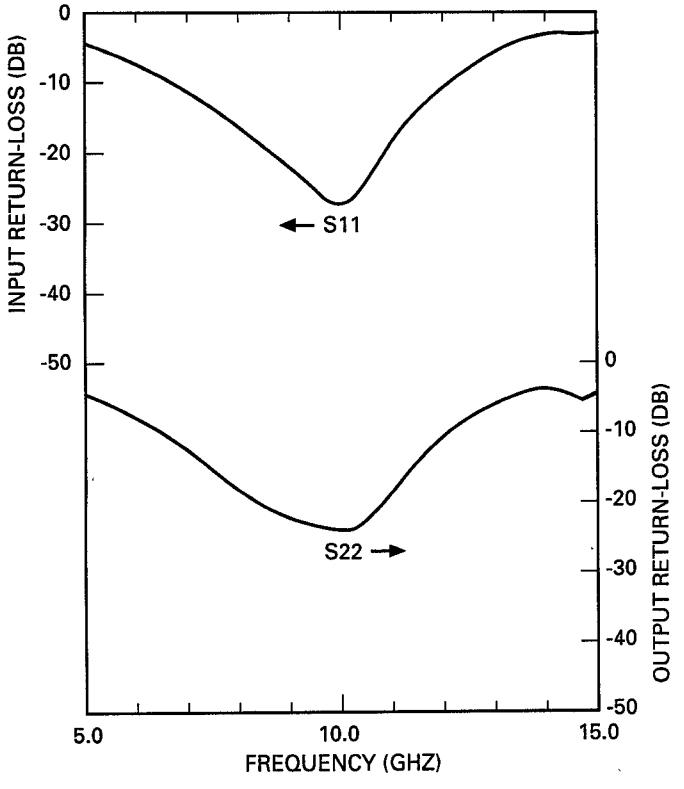


Fig. 20. Input and output return-loss performance of the *X*-band switch.

technology [15]. The reported GaAs p-i-n technology does a 3-μm thick intrinsic region which reduces the off-capacitance of the p-i-n diode. This GaAs p-i-n technology does not, however, integrate HBT transistors. The 1-dB bandwidth of the HBT p-i-n diode *X*-band switch is 35% and is limited by the bandwidth of the quarter-wave transformers. The "off" isolation is about 25 dB. This is relatively poor in comparison to the GaAs p-i-n technology referenced above, which can achieve 55 dB of isolation. The low HBT p-i-n switch isolation was found to be caused by high series ohmic contact resistance on the

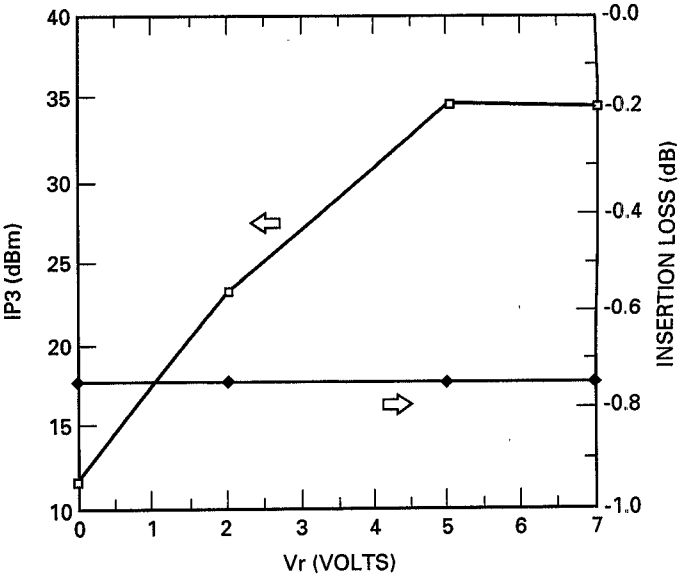


Fig. 21. IP3 performance at 10 GHz as a function of p-i-n diode reverse bias of the "on" arm.

measured wafers. Preliminary measurements on other wafers show isolations as high as 37 dB. The input and output return losses at 10 GHz are better than 15 dB and are shown in Fig. 20.

The IP3 was found to be dependent on the reverse bias of the p-i-n diode in the "on" arm. The IP3 was measured for various reverse bias voltages of the shunt p-i-n diode. Fig. 21 illustrates that for greater reverse biases, the IP3 improves. At a reverse bias of 7 V the IP3 was +34.5 dBm. The IP3 was not measured for higher reverse biases because of the limitations of our measurement system (35 dBm). The reverse bias breakdown is around 20 V for these p-i-n diodes.

IV. Conclusion

P-i-n diode attenuation, variable gain control, and switching functions were demonstrated using a self-aligned base ohmic metal AlGaAs/GaAs HBT technology. A wideband p-i-n diode variable gain amplifier achieved 14.6 dB gain, 9 GHz bandwidth, 15 dB of gain control, and a two-tone IP3 of $\geq$28 dBm at maximum gain. A two-stage p-i-n diode attenuator operating from 1–10 GHz was demonstrated with a minimum insertion loss of 3.7 dB, an attenuation range greater than 50 dB, and a maximum IP3 of 9 dBm. An *X*-band SPDT switch was also demonstrated with a minimum insertion loss of 0.82 dB, greater than 35% bandwidth, an off isolation of 25 dB, and an IP3 of at least 34.5 dBm. The p-i-n diodes were constructed from existing MBE layers of a base-line HBT process with no additional optimization of the process or material growth.

Acknowledgment

The authors acknowledge the support of S. Liang for modeling the HBT p-i-n diodes, K. W. Chang, R. Parish, S. Andrews for technical discussions on the design of the

p-i-n attenuator, and F. Oshita for measurement support on the IP3 measurements.

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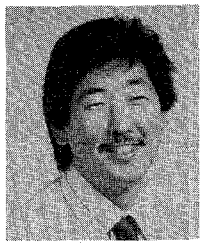

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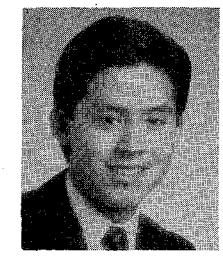

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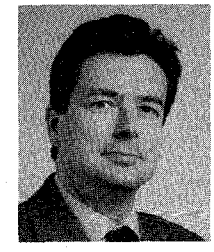

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